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EXAMINER
PEREZ RAMOS, VANESSA

ART UNIT	PAPER NUMBER
1765	5

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/706,043	Applicant(s) RYAN, ERROL TODD
	Examiner Vanessa Perez-Ramos	Art Unit 1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-123* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-123* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-23 and 45-57 and 59-100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dai (U.S. 5,877,076) in view of Liou et al. (U.S. 5,847,460) in further view of Wolf, S. "Silicon Processing for the VLSI Era", vol. 2, pp.20-27.

In regard to claims 1-5, 15-18, 21-23 and 45-56, Dai discloses a method comprising: forming a dielectric layer, which reads on Applicant's "process layer" (col. 5, lines 46-50 and Fig. 3c, layer "120"); forming a SiN layer, which reads on Applicant's "cap layer" over the dielectric or "process layer" (col. 5, lines 63-64, and Fig. 3C, layer "130"); forming a photoresist layer above the SiN or "cap" layer (col. 6, lines 19-21 and Fig. 3C, layer "150"); forming an opening in the photoresist layer (col. 6, line 35, and Fig. 3C, reference number "151"); etching into the SiN layer (col. 7, lines 14-26, and Fig. 3g, reference number "151"); removing the photoresist (col. 8, line 36, and Fig. 3j); and, performing a second etch to form an etch pattern in the dielectric or "process" layer (col. 7, lines 26-42, and Figs. 3i-3j).

Unlike the claimed invention, Dai does not disclose that the etching steps are anisotropic etching steps, nor does he disclose that a portion of the second process layer remains after etching the first process layer.

Liou teaches a semiconductor manufacturing process, discloses that, when etching openings, anisotropic etch procedures have many advantages over other etching procedures,

including the ability to form substantially vertical sidewalls and achieving better definition of small feature sizes on circuits.

Wolf teaches that, during semiconductor manufacturing, it is a well known practice to deposit a first process layer (p. 21, lines 1-2), followed by the deposition of a silicon nitride layer (p. 21, lines 17-18). A first etching process takes place, wherein the silicon nitride is etched (p. 22, line 23), and portions of this layer remain (p. 27, line 1).

It is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dai by specifically utilizing anisotropic etching, as per Liou, because anisotropic etching has many advantages over other etching methods, as disclosed by Liou, which are extremely desirable during semiconductor manufacturing. Furthermore, it would have been obvious to modify Dai by leaving a portion of the "second process layer" after the first etching step, as per Wolf, because this is the standard procedure in the art of semiconductor manufacturing.

In regard to claims 6-7, Dai discloses the formation of a second dielectric layer between the SiN or "cap" layer and the photoresist layer, which reads on Applicant's "anti-reflective coating", and which is etched during the first anisotropic etch.

In regard to claims 8-11 and 19-20, even if not disclosed by Dai, it is the Examiner's position that the removal of the anti-reflective and cap layers by CMP would have been obvious to one of ordinary skill in the art at the time of the invention, because these are well known steps and methods in the art of semiconductor manufacturing.

In regard to claim 13, the use of the claimed materials would have been obvious to one of ordinary skill in the art at the time of the invention, because they are all well known in the art of semiconductor manufacturing.

In regard to claim 14, removing layers by ashing would have been obvious to one of ordinary skill in the art at the time of the invention, because this is a well known procedure in the art of semiconductor manufacturing.

In regard to claim 57, the use of electroplating processes would have been obvious to one of ordinary skill in the art at the time of the invention, because this is a well known procedure in the art of semiconductor manufacturing.

In regard to claims 59-77, these claims differ from claims 1-23 above by adding the limitation that a second photoresist is deposited, and that a third etching step is performed.

Dai discloses the deposition of a second photoresist layer over the first photoresist (col.6, lines 55-57)

Even though Dai is silent about a third etching step, Dai does etch the "process" or dielectric layer as part of his second etching process.

It is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dai by utilizing more than two etching steps, in anticipation of an expected result (i.e., successfully etching the "process" or dielectric layer).

In regard to claims 78-100, these claims differ from claims 59-77 above by adding the limitation that a second "cap" layer is deposited over the first.

Dai is silent about the deposition of a second cap layer. However, Dai does disclose that the use of silicon nitride films (which read on Applicant's "cap" layers) is advantageous during semiconductor manufacturing, as it allows for a selective etch process with respect to underlying materials.

In view of Dai's disclosure regarding the advantages of SiN, it is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to

modify Dai by utilizing more than one SiN layer, with the expectation of achieving the highest possible degree of selectivity during etching.

3. Claims 24-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dai (U.S. 5,877,076) in view of Liou et al. (U.S. 5,847,460) in further view of Wolf, S. "Silicon Processing for the VLSI Era", vol. 2, pp.20-27, as applied to claims 1-23 and 45-57 above, and further in view of Chiang et al. (U.S. 5,817,572).

In regard to claims 24-44 and 58, these claims differ from claims 1-23 and 45-57 above by adding the limitations that: an opening is etched in the dielectric layer, a barrier layer is formed above the sidewall of said opening, and, a conductive material is formed in said opening.

Dai in view of Liou discloses the formation of an opening in the dielectric material (col. 7, lines 14-26, and Fig. 3g) and forming a conductive material in said opening (col. 7, lines 46-50, and Fig. 3K).

Unlike the claimed invention, Dai in view of Liou is silent about the formation of a barrier layer.

Chiang teaches a semiconductor manufacturing process that includes a step of forming a n opening, filling it with a barrier layer that includes titanium nitride and then with a conductive layer, and further discloses that the barrier layer functions to separate the dielectric material from the conductive material, acting as a "diffusion barrier" (col. 5, line 67, col. 6, lines 1-10, and col. 8, lines 59-67).

It is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dai in view of Liou by utilizing a barrier layer above the sidewall of the opening in the dielectric layer,. as per Chiang, because this results in improved

separation between the dielectric and conductive materials, which is extremely desirable during semiconductor manufacturing.

4. Claims 101-123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dai (U.S. 5,877,076) in view of Liou (U.S. 5,847,460) in further view of Wolf, S. "Silicon Processing for the VLSI Era", vol. 2, pp.20-27, as applied to claims 1-23, 45-56 and 58-100 above, and further in view of Nguyen (U.S. 5,821,169).

In regard to claims 101-123, these claims differ from claims 1-23, 45-56 and 58-100 above by adding the limitation that a hard mask layer is deposited between first and second dielctric layers, the hard mask layer having a n opening therein.

Dai in view of Liou is silent about the deposition of a hard mask layer between dielectric layers.

Nguyen teaches a semiconductor manufacturing method wherein a hard mask is deposited over a dielectric layer, and wherein the hard mask has at least one opening to reveal an integrated circuit area (col. 4, lines 46-67). Nguyen discloses that hard mask layers have been used to alleviate the effects of faceting in the transfer of a photoresist pattern to an interlevel dielectric. A hard mask profile can further improve the etch and via wall profiles etched into an interlevel dielectric (col. 2, line 66 thru col. 4, line 29).

It is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dai in view of Liou by utilizing a hard mask layer having an opening, as per Nguyen, because the use of hard mask layers has many advantages, including an improved finished product, which is extremely desirable during semiconductor manufacturing.

Response to Arguments

5. Applicant's arguments with respect to claims 1-123 have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vanessa Perez-Ramos whose telephone number is 703-306-5510. The examiner can normally be reached on Mon-Thurs 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703-308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5665.

Vanessa Perez-Ramos
Examiner
Art Unit 1765

VPR
December 16, 2002

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
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